Amendments to the Claims:

Please add new claims 9-14 as follows. Please amend claims 1 and 5 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A method of manufacturing a semiconductor device having a first region, in which a capacitance component is a dominant cause of a RC delay, and a second region, in which a resistance component is a dominant cause of a RC delay, comprising:

performing a first etching process to an insulating layer formed on a semiconductor substrate, so that [[a]]at least one first trench having a first ~~thickness~~ depth and a second trench having the first ~~thickness~~ depth are formed in the first region and the second region, respectively;

performing a second etching process to the second trench, so that a third trench having a second ~~thickness thicker~~ depth deeper than the first ~~thickness~~ depth is formed in the second region, wherein the insulating layer has a first thickness under the third trench and a second thickness under the at least one first trench, the first thickness of the insulating layer under the third trench being less than the second thickness of the insulating layer under the at least one first trench;

filling the at least one first trench and the third trench with a metal layer; and

removing portions of the metal layer, so that a first metal interconnection and a second metal interconnection are formed inside of the at least one first trench and the third trench, respectively.

2. (Original) The method of claim 1, wherein the metal layer is formed using copper.

3. (Original) The method of claim 2, wherein the metal layer of copper is formed using an electroplating method.

4. (Original) The method of claim 1, wherein the portions of the metal layer are removed using chemical mechanical polishing (CMP).

5. (Currently Amended) A method of manufacturing a semiconductor device having a first region, in which a capacitance component is a dominant cause of a RC delay, and a second region, in which a resistance component is a dominant cause of a RC delay, comprising:

forming a mask layer on an insulating layer formed on a semiconductor substrate;

forming a first photoresist layer pattern on the mask layer, so that a portion of the mask layer formed in the first region and a portion of the mask layer formed in the second region are exposed;

performing a first etching process using the first photoresist layer pattern as an etching mask, so that a mask layer pattern, in which the first region and the second region are exposed, is formed, and [[a]]at least one first trench having a first ~~thickness~~ depth and a second trench having the first ~~thickness~~ depth are formed in the first region and the second region, respectively;

removing the first photoresist layer pattern;

forming a second photoresist layer pattern, [[with]] by which the at least one first trench of the first region is covered and [[in]]by which the second trench and portions of the mask layer pattern are exposed;

performing a second etching process using the second photoresist layer pattern and the mask layer pattern as an etching mask, so that a third trench having a second ~~thickness thicker~~ depth deeper than the first ~~thickness~~ depth is formed in the second region, wherein the insulating layer has a first thickness under the third trench and a second thickness under the at least one first trench, the first thickness of the insulating layer under the third trench being less than the second thickness of the insulating layer under the at least one first trench;

removing the second photoresist layer pattern;

filling the at least one first trench and the third trench with a metal layer; and

removing portions of the metal layer, so that a first metal interconnection and a second metal interconnection are formed inside of the at least one first trench and the third trench, respectively.

6. (Original) The method of claim 5, wherein the metal layer is formed using copper.

7. (Original) The method of claim 6, wherein the metal layer of copper is formed using an electroplating method.

8. (Original) The method of claim 5, wherein the portions of the metal layer are removed using chemical mechanical polishing (CMP).

9. (New) The method of claim 1, wherein the first region is formed on a first side and a second side of the second region, and wherein a trench of the at least one first trench is formed in the first region at each of the first side and the second side of the second region.

10. (New) The method of claim 9, wherein each trench of the at least one first trench has the first depth, and wherein when the second etching process is performed to the second trench, the third trench has the second depth that is deeper than the first depth of each trench of the at least one first trench.

11. (New) The method of claim 9, wherein the insulating layer has a first thickness under the third trench and a second thickness under each trench of the at least one first trench, the first thickness of the insulating layer under the third trench being less than the second thickness of the insulating layer under each trench of the at least one first trench.

12. (New) The method of claim 5, wherein the first region is formed on a first side and a second side of the second region, and wherein a trench of the at least one first trench is formed in the first region at each of the first side and the second side of the second region.

13. (New) The method of claim 12, wherein each trench of the at least one first trench has the first depth, and wherein when the second etching process is performed to the second trench, the third trench has the second depth that is deeper than the first depth of each trench of the at least one first trench.

14. (New) The method of claim 12, wherein the insulating layer has a first thickness under the third trench and a second thickness under each trench of the at least one first trench, the first thickness of the insulating layer under the third trench being less than the second thickness of the insulating layer under each trench of the at least one first trench.